What is claimed is:

1. A nonvolatile memory comprising:

a memory cell array including:

a data storage area configured to store a data; and

a data invert flag storage area configured to store a data invert flag indicating whether or not the data is inverted,

the memory cell array configured to output selected data and a data invert flag related to the selected data;

a state machine configured to determine whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than a predetermined number when writing data into the memory cell array, the state machine configured to instruct a data controller to transfer inverted data and a data invert flag if it is equal to or greater than the predetermined number; and

the data controller configured to receive the data to be written into the memory cell array, the data controller configured to transfer, to the memory cell array, the data inverted according to the instruction of the state machine and the data invert flag.

2. The nonvolatile memory of claim 1, wherein the data storage area is arranged on column bit lines and the data invert flag storage is arranged on column bit lines that are different from those for the data storage.

3. The nonvolatile memory of claim 1, wherein the data invert flag storage is arranged for each of addresses related to the data storage.

4. The nonvolatile memory of claim 1, wherein the data invert flag storage area is arranged for a plurality of addresses related to the data storage.

5. The nonvolatile memory of claim 1, wherein when determining whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than the predetermined number, the state machine instructs, if the number is equal to or greater than a half of the number of bits of the data to write, the data controller to transfer, to the memory cell array, inverted data and a data invert flag indicating that the data is inverted.

6. The nonvolatile memory of claim 1, wherein when determining whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than the predetermined number, the state machine refers to a write current supply capacity of an internal power controller provided for the nonvolatile memory, and according to the determination, instructs the data controller to transfer, to the memory cell array, inverted data and a data invert flag

indicating that the data is inverted.

7. A nonvolatile memory comprising:

a memory cell array having a plurality of arrayed memory cells including:

data storage cells configured to store data; and

a data invert flag storage cell configured to store a data invert flag indicating whether or not the data is inverted,

the memory cell array configured to output selected data and a data invert flag related to the selected data;

a row decoder configured to select a word line of the memory cell array related to the data;

a column decoder configured to select bit lines of the memory cell array related to the data;

a data controller configured to receive the data to be stored in the memory cell array, the data controller configured to transfer the data, or inverted data and the data invert flag related to the data to the memory cell array, the data controller configured to provide a write bit line voltage through the column decoder to corresponding memory cells in the memory cell array when transferring;

a state machine configured to determine whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than a predetermined number, when writing the data into the memory cell array, the state

machine configured to instruct a data controller to transfer inverted data and the data invert flag if it is equal to or greater than the predetermined number; and

a sense amplifier connected to bit lines of the memory cell array through the column decoder, the sense amplifier configured to invert, in a data read operation, selected data according to a data invert flag related to the selected data and output the inverted data.

8. The nonvolatile memory of claim 7, wherein the data storage is arranged on column bit lines and the data invert flag storage is arranged on column bit lines that are different from those for the data storage.

9. The nonvolatile memory of claim 7, wherein the data invert flag storage is arranged for each of addresses related to the data storage.

10. The nonvolatile memory of claim 7, wherein the data invert flag storage area is arranged for a plurality of addresses related to the data storage.

11. The nonvolatile memory of claim 7, wherein when determining whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than the predetermined number, the state machine instructs, if the

number is equal to or greater than a half of the number of bits of the data to write, the data controller to transfer, to the memory cell array, inverted data and a data invert flag indicating that the data is inverted.

12. The nonvolatile memory of claim 7, wherein when determining whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than the predetermined number, the state machine refers to a write current supply capacity of an internal power controller provided for the nonvolatile memory, and according to the determination, instructs the data controller to transfer, to the memory cell array, inverted data and a data invert flag indicating that the data is inverted.

13. A nonvolatile memory comprising:

a memory cell array having a plurality of arrayed memory cells including:

data storage cells configured to store data; and

a data invert flag storage cell configured to store a data invert flag indicating whether or not the data is inverted, the data storage cells and the data invert flag storage cell corresponding to the data storage cells is in the same row, the memory cell array configured to output selected data and a data invert flag related to the selected data;

a row decoder configured to select a word line of the memory cell array related to the data;

a column decoder configured to select a bit line of the memory cell array related to the data;

an internal power controller configured to control a voltage applied to the memory cell array;

a protect register configured to store write-protect information concerning a given storage place in the memory cell array;

a command interface configured to receive a command related to an operation of the nonvolatile memory;

a state machine configured to receive, in response to an operation instruction from the command interface, write-protect information from the protect register, the state machine configured to determine a state of a data storage cell in the memory cell array related to a write target address, the state machine configured to obtain write data from a data controller if it is determined that the data storage place is writable, the state machine configured to determine whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than a predetermined number when writing the data in the memory cell array, the state machine configured to instruct a data controller to transfer inverted data and a data invert flag if it is greater than the predetermined number;

the data controller configured to receive the data to be stored in the memory cell array, the data controller configured to transfer data inverted according to the instruction from the state machine and the data invert flag related to the inverted data to the memory cell array, the data controller configured to supply a write bit line voltage from the internal power controller through the column decoder to the target memory cells in the memory cell array; and

a sense amplifier connected to bit lines of the memory cell array through the column decoder, the sense amplifier configured to invert, in a data read operation, selected data according to a data invert flag related to the selected data and output the inverted data.

14. The nonvolatile memory of claim 13, wherein the data storage is arranged on column bit lines and the data invert flag storage is arranged on column bit lines that are different from those for the data storage.

15. The nonvolatile memory of claim 13, wherein the data invert flag storage is arranged for each of addresses related to the data storage.

16. The nonvolatile memory of claim 13, wherein the data invert flag storage area is arranged for a plurality of addresses related to the data storage.

17. The nonvolatile memory of claim 16, wherein in response to an operation instruction from the command interface, the state machine receives write protect information from the protect register, determines states of a plurality of storage places at write target addresses, if it is determined that all of these storage places are writable, obtains a plurality of write data pieces from the data controller, determines, when writing the plurality of write data pieces in the memory cell array, whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than a predetermined number, and if it is equal to or greater than the predetermined number, instructs the data controller to transfer, to the memory cell array, inverted ones of the plurality of write data pieces and a data invert flag indicating that the data pieces are inverted.

18. The nonvolatile memory of claim 13, wherein when determining whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than the predetermined number, the state machine instructs, if the number is equal to or greater than a half of the number of bits of the data to write, the data controller to transfer, to the memory cell array, inverted data and a data invert flag indicating that the data is inverted.

19. The nonvolatile memory of claim 13, wherein when determining whether or not the number of memory cells to which a bias voltage is applied is equal to or greater than the predetermined number, the state machine refers to a write current supply capacity of an internal power controller provided for the nonvolatile memory, and according to the determination, instructs the data controller to transfer, to the memory cell array, inverted data and a data invert flag indicating that the data is inverted.

20. The nonvolatile memory of claim 13, wherein the nonvolatile memory is a NOR flash memory.